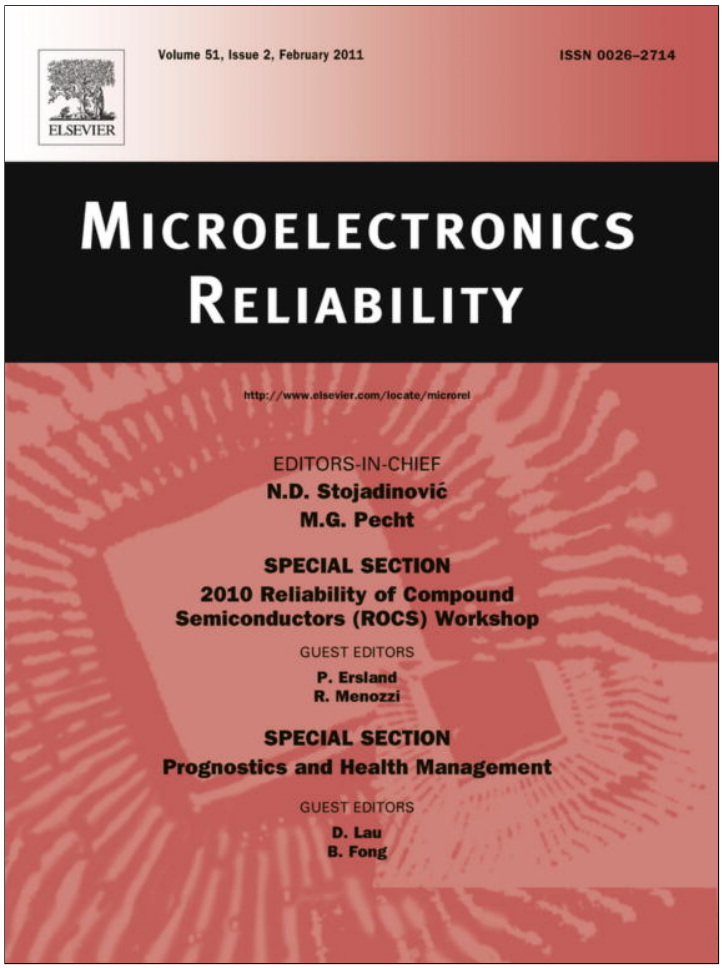

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Electrical characterization of MS and MIS structures on AlGaN/AlN/GaN heterostructures

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ABSTRACT

The forward and reverse bias *I–V*, *C–V*, and G/ω–*V* characteristics of (Ni/Au) Schottky barrier diodes (SBDs) on the $Al_{0.22}Ga_{0.78}N$/AlN/GaN high-electron-mobility-transistor (HEMTs) without and with SiN_x insulator layer were measured at room temperature in order to investigate the effects of the insulator layer (SiN_x) on the main electrical parameters such as the ideality factor (n), zero-bias barrier height (Φ_{B0}), series resistance (R_s), interface-state density (N_{ss}). The energy density distribution profiles of the N_{ss} were obtained from the forward bias *I–V* characteristics by taking into account the voltage dependence of the effective barrier height (Φ_e) and ideality factor (n_V) of devices. In addition, the N_{ss} as a function of E_c–E_{ss} was determined from the low-high frequency capacitance methods. It was found that the values of N_{ss} and R_s in SBD HEMTs decreases with increasing insulator layer thickness.

1. Introduction

$Al_xGa_{1-x}N$/GaN heterostructures have attracted much regard for their important applications for high-speed, high-power, and high-temperature electronic devices [1–3]. One of the important problem of the nitride-based high-power microwave electronics is the presence of trapping centers resulting from deep defects and/or impurities in the materials. This trapping centers leads to high leakage current. The relatively slow charging and discharging of these defect states, with time constants in the microseconds range, cause $Al_xGa_{1-x}N$/GaN HEMTs to experience RF dispersion and leakage current [1–5]. In order to reduce RF dispersion and leakage current the AlGaN surface can be passivated with dielectric materials. The most commonly reported one is the SiN_x deposited by PECVD [4,5]. Various passivation materials have been reported to control surface states and decrease a leakage current of AlGaN/GaN HEMTs [6,7]. The fundamental requirements for the materials are high dielectric constant [3–16]. The interface quality between the deposited metal and the semiconductor surface decides the performance and reliability of these devices. Therefore, in order to reduce the leakage current and interface-state density, a variety of gate oxides/insulators such as Al_2O_3 [3,6,7], ZrO_2 [9], SiN_x [4,5,10], $SrTiO_3$ [12], $Bi_3Ti_4O_{12}$ [14], HfO_2 [15], and SiO_xN_y [16] materials have been proposed for application as an insulator layer at the metal/semiconductor (M/S) interface in semiconductor devices such as a metal–insulator–semiconductor (MIS) or metal–oxide–semiconductor (MOS), metal–ferroelectric–semiconductor (MFS) or metal–ferroelectric–insulator–semiconductor (MFIS), metal–oxide–semiconductor field effect transistor (MOSFET), MFISFET structures and high-electron-mobility-transistors (HEMTs) [3–16].

The performance and reliability of Schottky gate AlGaN/GaN HEMTs are largely impaired by high gate leakage current [6] and the poor long-term reliability of the Schottky gate. Using a thin film between the metal and semiconductor, such as Si_3N_4, can not only prevent the reaction and inter-diffusion between the metal and AlGaN barrier layer, but can also further improve the retention properties [10,11]. In addition, the various non-idealities, such as the formation of an insulator layer at the M/S interface, the energy distribution profile of N_{ss} at the semiconductor/insulator (S/I) interface, R_s and inhomogeneous Schottky barrier heights (SBHs) all affect the electrical characteristics of MIS and HEMT structures.

The quality and the thickness of the insulator layer between metal and semiconductor are important parameters that affect the main electrical parameters [8,9,19–21]. In general, the forward bias *I–V* characteristics are linear in the semi-logarithmic scale at intermediate bias voltages (~0.1–0.8 V), but deviate from the linearity due to the effect of R_s when the applied-bias voltage is sufficiently large ($V \geqslant 0.8$ V) [4,10,17–21]. Since a bias voltage is applied across these structures, the combination of the insulator layer, depletion layer, and series resistance of the device will share the applied-bias voltage. Therefore, the high values of the ideality factor of these structures can be explained by means of the effects of the bias voltage drop across the insulator layer, surface states, bias dependence of the barrier height (BH), and barrier inhomogeneity at the M/S interface. The first studies on the insulator layer at

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the M/S interface were conducted by Cowley and Sze [22], who obtained their estimations from an analysis of the Schottky barrier heights (SBHs) with different metallization as a function of the metal work function. Already, some studies [9,10,17,18] inspected the effect of existence of an insulator/oxide layer and the N_{ss} on the behavior of SBDs, and extracted the density distribution of N_{ss} in the semiconductor band gap from the forward bias I–V characteristics.

The aim of the present study is to compare some of the main electrical parameters of SBD HEMTs and MIS HEMTs by using I–V, C–V, and G/ω–V measurements at room temperature. In order to determine the energy density distribution of the N_{ss} was obtained from the forward bias I–V characteristics by taking into account the bias dependence of the effective BH (Φ_e) and n_V, as well as low–high frequency C–V characteristics. In addition, the values of R_s of these structures were determined from forward bias I–V by using Cheung's functions.

2. Experimental procedure

The $Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures on c-plane (0 0 0 1) double-polished 2-in. diameter Al_2O_3 substrate in a low-pressure metalorganic chemical-vapor deposition (MOCVD) reactor (Aixtron 200/4 HT-S) by using trimethylgallium (TMGa), trimethylaluminum (TMAl), and ammonia as Ga, Al, and N precursors, respectively. Prior to the epitaxial growth, Al_2O_3 substrate was annealed at 1100 °C for 10 min in order to remove surface contamination. The buffer structures consisted of a 15 nm thick, low-temperature (650 °C) AlN nucleation layer along with high temperature (1150 °C) 420 nm AlN templates. A 1.6 μm nominally undoped (ud) GaN layer was grown on an AlN template layer at 1050 °C, which was followed by a 2 nm thick high temperature undoped AlN (1150 °C) barrier layer. After the deposition of these layers, a 23 nm thick undoped $Al_{0.22}Ga_{0.78}N$ layer was grown at 1050 °C. Finally, a 5 nm thick undoped GaN cap layer growth was carried out at a temperature of 1085 °C.

The grown wafers were cut into several pieces and the ohmic and Schottky/rectifier contacts were made atop the sample in the high vacuum coating system at approx. 10^{-7} Torr.

For the Hall effect measurements by the van der Pauw method, square shaped (5×5 mm^2) samples were prepared with four evaporated triangular in the corners and the Schottky contacts were formed as 1 mm diameter circular dots (Fig. 1). Prior to ohmic contact formation, the samples were cleaned with acetone in an ultrasonic bath. Then, samples were treated with boiling isopropyl alcohol for 5 min and rinsed in de-ionized (DI) water having 18 MΩ resistivity. After cleaning, the samples were dipped in a solution of HCl/H_2O (1:2) for 30 s in order to remove the surface oxides, and were then rinsed in DI water again for a prolonged period. Ti/Al/Ni/Au (16/180/50/150 nm) metals were thermally evaporated on the sample and were annealed at 850 °C for 30 s in N_2 ambient in order to form the ohmic contact.

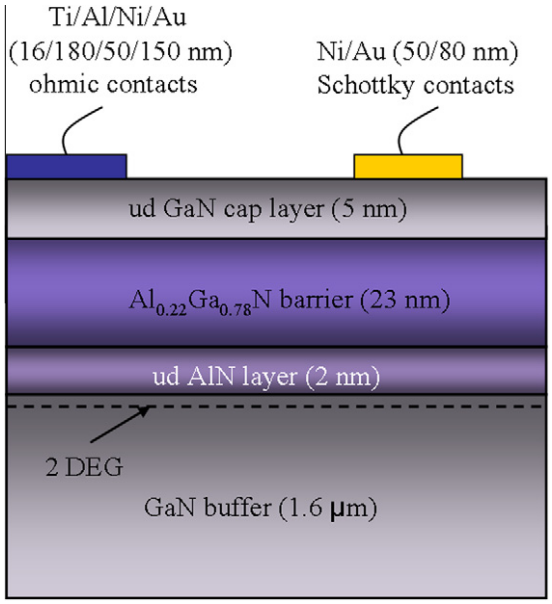

Fig. 1. Schematic diagram of the $Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructure and view of ohmic and Schottky contact on the structures.

After the formation of the ohmic contact, the SiN_x layer was deposited by plasma-enhanced chemical-vapor deposition (PECVD) on $Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures at 300 °C. The SiN_x growth was optimized to have a low growth rate without changing the refractive index by a series of growth and ellipsometric measurements. After growth rate optimization, we achieved growth rate of about 10 nm/min with a refraction index of 2.02. And 5.5 nm and 11 nm thick SiN_x layers were deposited on samples B and C, respectively. We were able to measure the SiN_x thickness exactly with ellipsometer. Sample A, however, did not have any passivation layer. Finally, 1 mm diameter Schottky contact areas were defined by Ni/Au (50/80 nm) evaporation using a hard mask.

The current–voltage (I–V) measurements were performed by the use of a Keithley 2400 SourceMeter. The capacitance voltage (C–V) and conductance voltage (G/ω–V) measurements were performed at 1 MHz by using HP 4192A LF impedance analyzer (5 Hz–13 MHz). All measurements were carried out at room temperature in the Janes vpf-475 cryostat and with the help of a microcomputer through an IEEE-488 AC/DC converter card. The surface morphology was characterized by atomic force microscope (AFM).

3. Results and discussion

3.1. Forward and reverse bias I–V characteristics

Fig. 2 shows AFM image of the surface of the SBD HEMTs and MIS HEMTs. The AFM image (2×2 μm^2) of the surface shows wavy surface with root mean square (rms) roughness of 0.33, 1.27 and 1.33 nm for sample A, sample B and sample C, respectively. The rms value of the surface roughness was increased with increasing SiN_x layer thickness.

The forward and reverse bias current–voltage (I–V) characteristics of the (Ni/Au) Schottky barrier diodes on the $Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures without and with SiN_x insulator layer were investigated at room temperature. Fig. 3 compares the forward and reverse bias semi-logarithmic $ln\,I$–V characteristics of two MIS HEMTs with 5.5 nm and 11 nm SiN_x insulator layer and SBD HEMTs samples. The measurements results confirm a significant reduction in leakage current of about four orders of magnitude for the MIS HEMTs, with 11 nm SiN_x insulator layer, in comparison to the SBD HEMTs. It is noted that in the positive bias region is also significantly reduced by SiN_x insulator layers. Also the SiN_x insulator is effective in suppressing not only the leakage current but also in enhancing the forward turn-on voltage, as shown in Fig. 3. Therefore growing a high quality SiN_x layer as the insulator will suppress the leakage current to a large extent and possibly shift the device threshold voltage [10].

In general, the relationship between the applied-bias voltage ($V \geqslant 3$ kT/q) and the current through a barrier between the metal and semiconductor of the MS, MIS, and solar cells, with series resistance, is given by [17]

$$I = \underbrace{AA^*T^2 \exp\left(-\frac{q\Phi_{B0}}{kT}\right)}_{I_0} \exp\left[\left(\frac{q(V-IR_s)}{nkT}\right)-1\right] \quad (1)$$

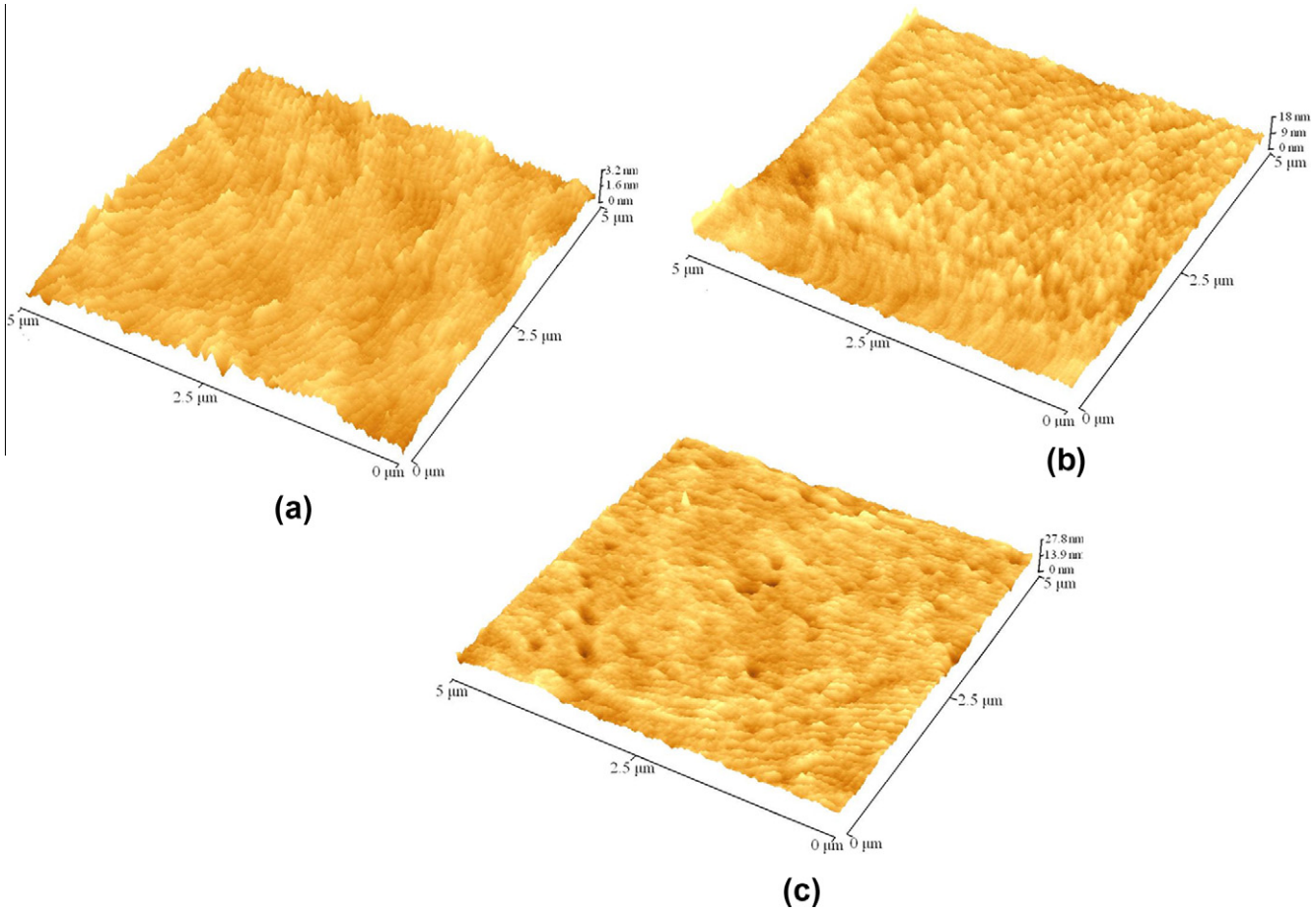

Fig. 2. AFM image ($2 \times 2\ \mu m^2$) showing the surface morphology of the (a) SBD HEMTs (sample A) and MIS HEMTs (b) sample B and (c) sample C.

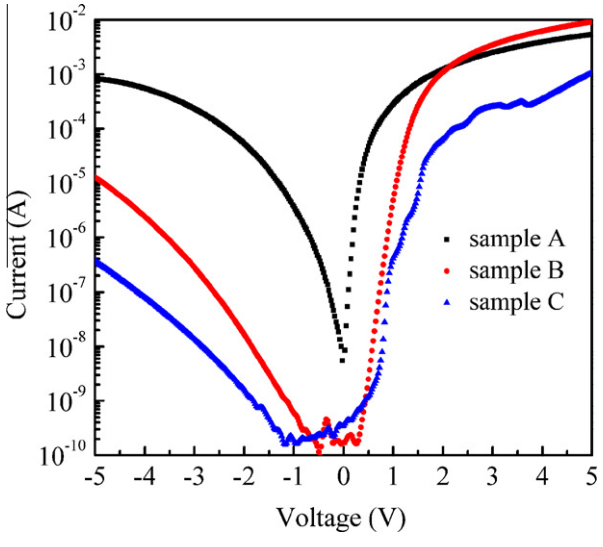

Fig. 3. Forward and reverse bias semi-logarithmic *ln I–V* characteristics of SBD HEMTs and MIS HEMTs.

where Φ_{B0} is the zero-bias barrier height, A is the rectifier contact area, A^* is the effective Richardson constant and is equal to 32.09 A/cm^2 K^2 for undoped $Al_{0,22}Ga_{0,78}N$ [23], in which I_0 is the reverse saturation current derived from the straight line intercept of *ln I* at zero bias voltage [17]. The term IR_s is the voltage drop across the series resistance of the diode. The voltage $V_d = V - IR_s$ across the diode can be expressed in terms of the total voltage drop V across the series combination of the diode and the series resistance. In Eq. (1), n is the ideality factor, T is the absolute temperature in Kelvin, k is the Boltzmann constant, V is the applied voltage across the structure.

The value of n can be derived from the slope of *ln I* vs V plot [17–19]. Each *ln I–V* curve consists of a linear range with different slopes. The n values for SBD HEMTs (sample A) and MIS HEMTs (sample B and sample C) were obtained as 1.5, 2.5 and 4.0, respectively. It is clear that the n values of the heterostructure are larger than unity and its values increases with increasing insulator layer thickness (Table 1). These values of the ideality factors show that the structures follow an MIS configuration rather than MS SBDs [13,18–20,24]. Such behavior of n can especially be attributed to the existence of an insulator layer, a wide distribution of low BH patches, a tunneling mechanism, and the particular distribution of N_{ss} at the M/S interface [9,17–26]. In general, the semiconductor surface is inevitably covered with a native thin insulator layer if the semiconductor surface is prepared by the usual polishing and chemical etching, in which the evaporation of metal is carried out in a conventional vacuum system [18,27–29]. For a sufficiently thick interface insulator layer, the interface states are in equilibrium with the semiconductor, and they cannot interact with the metal [17–19,27,29].

The value of the saturation current I_0 was obtained by extrapolating the linear intermediate bias voltage region of the curve to zero applied-bias voltage, in which the zero bias BH (Φ_{B0}) value was calculated from Eq. (1) for each sample and is shown in Table 1. The downward curvature at sufficiently high bias voltages was caused by the effect of R_s, apart from the existence of the interface

Table 1
The passivation layer thickness dependent values of parameters determined from *I–V* characteristics of SBD HEMTs and MIS HEMTs.

Sample ID	n	I_0 (A)	Φ_B (*I–V*) (eV)	R_s ($dV/d\ln(I)$) (Ω)	R_s ($H(I)$) (Ω)
A	1.52	6.86×10^{-9}	0.73	665	653
B	2.54	1.03×10^{-12}	0.95	310	290
C	4.05	1.06×10^{-11}	0.89	383	352

states [17,19,25]. While the R_s, is significant especially in the downward curvature of the forward bias *I–V* characteristics, the N_{ss} is effective in the inversion and depletion regions, and their distribution profile changes from region to region in the band gap. For these reason, in this small linear region, the accuracy of the determination of the barrier height and n becomes poorer. Therefore, n, BH, and R_s were evaluated by using a method that was developed by Cheung and Cheung functions [25] in the high current range.

Eq. (1) can be rearranged as the following expressions [25].

$$\frac{dV}{d(\ln I)} = n\frac{kT}{q} + IR_s \tag{2a}$$

$$H(I) = V - n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\Phi_b \tag{2b}$$

where Φ_B is the barrier height obtained from the data of the downward curvature region in the forward bias *I–V* characteristics. Fig. 4a and b show the experimental $dV/d(\ln I)$ vs I and $H(I)$ vs I plots for all the samples obtained from the forward bias *I–V* data, respectively. As can be seen in Fig. 4a, $dV/d(\ln I)$ vs I gives a straight line for the data of the downward curvature region in the forward bias *I–V*. Thus, the plot of $dV/d(\ln I)$ vs I will give R_s as the slope and nkT/q as the y-axis intercept. Furthermore, from the Cheung and Cheung functions plot the n and R_s values that were obtained for all the samples at room temperature. The $H(I)$ functions were derived by using these n values in Eq. (2b). The plot of $H(I)$ vs I will also lead to a straight line (as shown in Fig. 4b) with a y-axis intercept that is equal to $n\Phi_B$. The slope of this plot also provides a second determination of R_s, which can be used to check the consistency of this approach. Thus, for all the samples and by performing different plots (Eq. (2a)) of the *I–V* data, the values of R_s are obtained and shown in Table 1. As shown in Table 1, the n values obtained from Eq. (1) and the average R_s obtained from both Eq. (2a) values by different techniques are in good agreement with each other. The series resistance differences between the samples can arise from some different sources: (1) the contact made by the probe wire to the gate (2) the ohmic to the AlGaN/AlN/GaN HEMT surface (3) difference in the thickness of SiN_x layer [26].

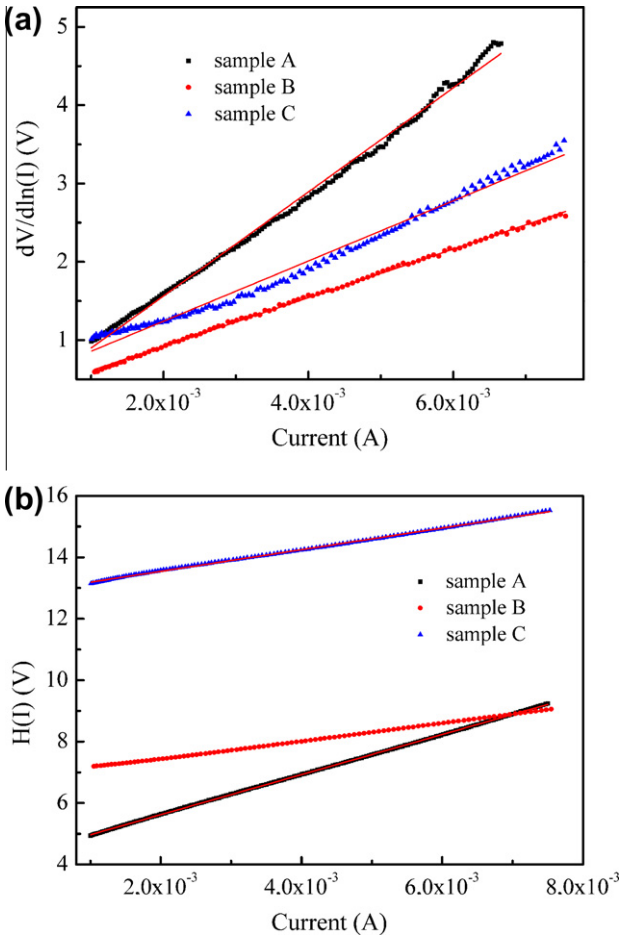

Fig. 4. The (a) $dV/d\ln I$ vs I and (b) $H(I)$ vs I characteristics of SBD HEMTs and MIS HEMTs obtained from the forward bias *I–V* data.

The voltage dependent ideality factor n_V can be written from Eq. (1) as:

$$n_V = \frac{qV}{kT\ln(I/I_0)} \tag{3}$$

In addition, the voltage dependence of the effective barrier height, Φ_e is contained in the ideality factor, n through the relation [18,24,27–30] as

$$\Phi_e = \Phi_{B0} + \beta V = \Phi_{B0} + \left(\frac{d\Phi_e}{dV}\right)V \tag{4}$$

where $d\Phi_e/dV$ is the change in the barrier with bias voltage. For the metal–insulator–semiconductor (MIS) diode having interface states that are in equilibrium with the semiconductor, the ideality factor n becomes greater than unity. As proposed by Card and Rhoderick [18], it is given by

$$n = \frac{q}{kT}\frac{dV}{d\ln I} = \frac{1}{(1 - d\Phi_{B0}/dV)} \tag{5}$$

Eq. (1) is often used to evaluate the *I–V* characteristics. However, this does not include the effects of the applied voltage on the barrier height. If $d\Phi_e/dV$ is constant, the ideality factor n should be constant, and the ideality factor n obtained Eq. (4) deviates from the experimental results. Furthermore, the following expression can be used for the ideality factor [19],

$$n = 1 + \frac{\frac{\delta}{\varepsilon_i}\left(\frac{\varepsilon_s}{W} + qN_{sb}\right)}{1 + \frac{\delta}{\varepsilon_i}q^2N_{sa}} \tag{6}$$

where N_{sb}, N_{sa} are the densities of the interface states that are in equilibrium with the metal and semiconductor, respectively. ε_s and ε_i are the permittivity of semiconductor and insulator layer, respectively. For the MIS type Schottky diodes, the interface states that are entirely governed by the semiconductor, the expression for the density of the interface states as deduced by Card and Rhoderick [18] can be reduced as

$$N_{ss} = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n-1) - \frac{\varepsilon_s}{W_D}\right] \tag{7}$$

where δ is the thickness of the insulator layer, and W_D is the depletion layer width that is being determined from the experimental *C–V* measurements at a sufficiently high frequency ($f \geqslant 1$ MHz). Here, the values of ε_i and ε_s used as $7.5\varepsilon_0$ and $8.9\varepsilon_0$ for SiN_x layer and AlGaN, respectively [31].

The energy of interface states E_{ss} with respect to the conductance band edge is given by [18–27]

$$E_c - E_{ss} = q(\Phi_e - V) \tag{8}$$

The energy density distribution profile of the interface states N_{ss} for (Ni/Au) SBDs on AlGaN/AlN/GaN heterostructures without and with SiN_x insulator layer were obtained from the experimental forward bias I–V and are shown in Fig. 5. As can be seen in Fig. 5, for all samples there was a slight exponential increase in N_{ss} from the nearly mid-gap towards the bottom of the conductance band. In this case, while the donor type N_{ss} is in effect near the conductance band, the acceptor type N_{ss} is in effect near the valance band. It is obvious that the values of N_{ss} decrease with the increase of the insulator layer thickness. Moreover, the densities of the interface states for sample A are in equilibrium with the metal, and the other samples (sample B and sample C) are in equilibrium with the semiconductor due to a sufficiently large insulator layer thickness.

3.2. Forward and reverse bias C–V and G/ω–V characteristics

Fig 6a and b show the C–V and G/ω–V measurements at 1 MHz and at room temperature for the (Ni/Au) SBDs on $Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures without and with SiN_x insulator layer. At sufficiently high frequencies ($f \geqslant 1$ MHz), the N_{ss} cannot follow the (ac) signal, because at high frequencies the carrier life time (τ) is larger than the measured period [26]. Therefore, the C–V and G/ω–V measurements were performed at 1 MHz. As can be seen in Fig. 6a, the C–V characteristics of the sample A, sample B and sample C exhibit inversion, depletion and accumulation regions. However, the behavior of the C–V curves is different for each region for each sample. The C–V characteristic of sample A shows two peaks in the inversion and accumulation region at about −8.3 V and −0.6 V, respectively. The first peak can be attributed to the interface states localized at M/S interface. However, the second peak can be explained with the effect of the R_s [26,32,33]. It is well know, the interface states are effective for the inversion and depletion region. On the other hand, series resistance of device is effective only in accumulation region or at sufficiently forward bias region [26,32,33]. In the recent studies, the existence of capacitance peak in the C–V plot is confirmed by the number of experimental results on MIS-Schottky barrier devices [32,33]. It has been shown that, in the presence of series resistance, the capacitance–voltage should exhibit a peak. The peak value of the capacitance depends on a number of parameters such as doping concentration, interface-state density and the thickness of the insulator layer [32–34]. Werner et al. [34], on the other hand, made

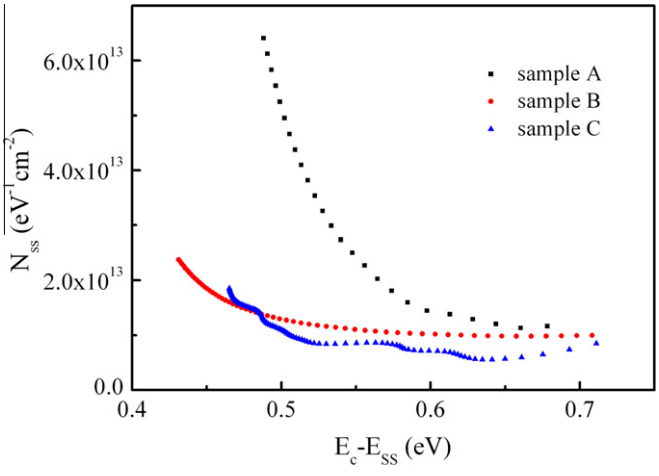

Fig. 5. Density of interface states N_{ss} as a function of E_c–E_{ss} deduced from the I–V data for SBD HEMTs and MIS HEMTs.

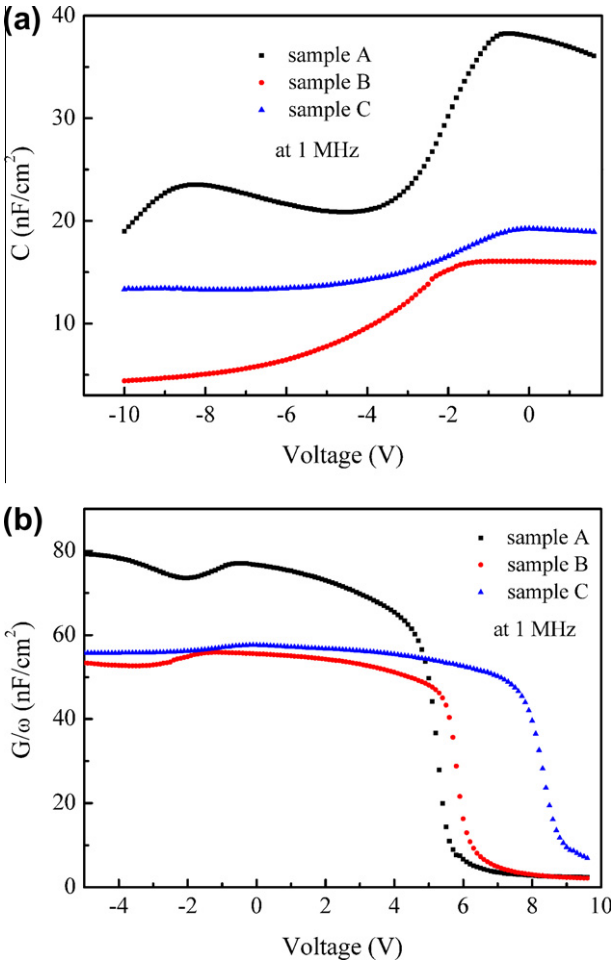

Fig. 6. The measured (a) C–V and (b) G/ω–V characteristics of SBD HEMTs and MIS HEMTs measured at 1 MHz.

a systematic investigation on several Schottky barrier devices with both ohmic and non-ohmic back contacts an correlated this anomalous variation in capacitance to non-ohmic back contact.

The density distribution profile of N_{ss} was also obtained from the low–high frequency capacitance measurements, as seen in the following equation [26]

$$N_{ss} = \frac{1}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{HF}} - \frac{1}{C_i}\right)^{-1}\right] \tag{9}$$

where C_{LF} and C_{HF} are the measurement low frequency capacitance (5 kHz) and high frequency capacitance (1 MHz), respectively, and C_i is the insulator layer capacitance. The capacitance of insulator layer (C_i) is calculated, from the accumulation capacitance, to be 327 nF/cm^{-2}, 283 nF/cm^{-2} and 194 nF/cm^{-2} for samples A, B and C, respectively. For sample A native oxide layer taken as insulator layer. It is well known that, unless specially fabricated, a Schottky barrier diode possesses a thin interfacial native oxide layer between the metal and semiconductor. The existence of such an insulating layer can have a strong influence on the diode characteristics. Consequently, there are several possible reasons of errors that cause deviation of the ideal behavior of with and without an insulator layer Schottky diodes and must be taken into account. These include the effects of insulator layer between metal and semiconductor, interface states (N_{ss}), series resistance (R_s), and formation of barrier height at MS interface. Also, in the presence of a series resistance, the C–V characteristics should exhibit a peak. The peak value of capacitance is found to vary with series resistance, inter-

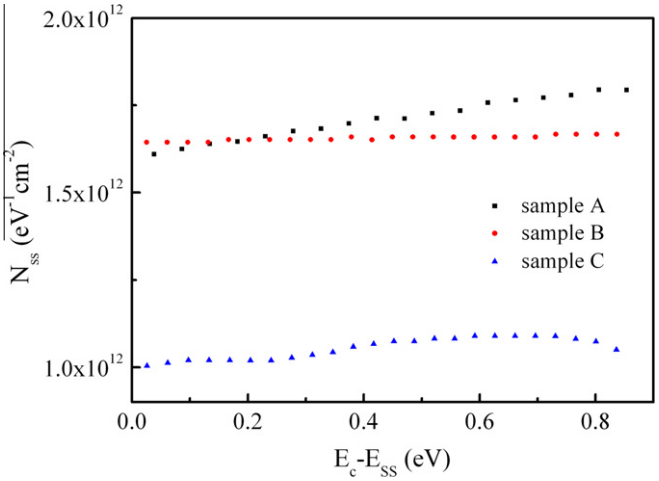

Fig. 7. Density of interface states N_{ss} as a function of E_c–E_{ss} deduced from the low–high frequency C–V data for SBD HEMTs and MIS HEMTs.

face-state density, and frequency of the ac signal [32,33]. The series resistance is an important parameter, which causes the electrical characteristics of MS and MIS-Schottky diodes to be non-ideal [12–17].

The advantage of this method comes from the fact that it enables the determination of the many properties of the insulator layer. In this method [26], the N_{ss} is extracted from its capacitance contribution to the measured experimental C–V curve. In the equivalent circuit of MIS type diodes, the C_i is in series with the parallel combination of the interface state capacitance and the space charge capacitance. At sufficiently high frequencies ($f \geqslant 1$ MHz), the interface states cannot respond to the ac excitation, so that they do not contribute to the total capacitance directly. Fig. 7 shows the density distribution profile of N_{ss}, which was obtained for all the samples. As can be seen in Fig. 7, the values of N_{ss} decrease with the increase of the insulator layer thickness.

4. Conclusions

In summary, the forward and reverse bias I–V, C–V, and G/ω–V characteristics of the SBDs on $Al_{0.22}Ga_{0.78}N$/AlN/GaN heterostructures without and with SiN_x insulator layer were measured in order to investigate the effects of the insulator layer on the main electrical parameters such as the ideality factor (n), zero-bias barrier height (Φ_{B0}), series resistance (R_s) and interface-state density (N_{ss}) at room temperature. The experimental results show that the values of the insulator layer thickness and R_s were found to strongly affect the function of the main electrical parameters. The values of R_s of these structures were obtained from Cheung's and conductance methods by using forward bias I–V characteristics. The energy distribution profile of N_{ss} was obtained from the forward bias I–V characteristics, by taking into account the bias dependence of the ϕ_e and n_V, as well as the low–high frequency C–V characteristics. It is obvious that the determined values of N_{ss} from I–V and low–high frequency capacitance methods decrease with the increase of the insulator layer thickness.

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