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Investigation of Trap States in AlInN/AlN/GaN Heterostructures by Frequency-Dependent Admittance Analysis

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We present a systematic study on the admittance characterization of surface trap states in unpassivated and SiN_x-passivated $Al_{0.83}In_{0.17}N$/AlN/GaN heterostructures. C–V and G/ω–V measurements were carried out in the frequency range of 1 kHz to 1 MHz, and an equivalent circuit model was used to analyze the experimental data. A detailed analysis of the frequency-dependent capacitance and conductance data was performed, assuming models in which traps are located at the metal–AlInN surface. The density (D_t) and time constant (τ_t) of the surface trap states have been determined as a function of energy separation from the conduction-band edge ($E_c - E_t$). The D_{st} and τ_{st} values of the surface trap states for the unpassivated samples were found to be $D_{st} \cong (4 - 13) \times 10^{12}$ $eV^{-1}cm^{-2}$ and $\tau_{st} \approx 3$ μs to 7 μs, respectively. For the passivated sample, D_{st} decreased to 1.5×10^{12} $eV^{-1}cm^{-2}$ and τ_{st} to 1.8 μs to 2 μs. The density of surface trap states in $Al_{0.83}In_{0.17}N$/AlN/GaN heterostructures decreased by approximately one order of magnitude with SiN_x passivation, indicating that the SiN_x insulator layer between the metal contact and the surface of the $Al_{0.83}In_{0.17}N$ layer can passivate surface states.

Key words: Capacitance, conductance, trap center, AlInN heterostructures, admittance

INTRODUCTION

AlGaN/GaN high-electron-mobility transistors (HEMTs) have been intensively studied as candidates for high-power devices, as well as high-speed and high-temperature operation.[1,2] In replacing the AlGaN barrier layer with an InAlN layer in the AlGaN/GaN structure, HEMTs in turn offer potentially higher sheet charge densities because of the higher spontaneous polarization of InAlN compared with AlGaN.[3,4] An important feature of the $Al_{1-x}In_xN$ alloy is the possibility to grow epitaxial layers that are lattice matched to GaN at an indium content x of ~17%.[4–6] For lattice-matched $Al_{0.83}In_{0.17}N$/AlN/GaN, the heterostructure interface minimizes strain, and thereby minimizes cracking and/or dislocation formation.[5,6] Because of this, AlInN/GaN-based HEMTs are superior to more conventional AlGaN/GaN HEMTs.[7,8] In general, the electrical charge trap states on the surface and/or in the bulk of the heterostructure change the density of the two-dimensional electron gas (2DEG) in the channel and, therefore, limit the electronic performance of those devices in operation through the trapping/detrapping process and decrease the carrier concentration and lower the drain current, transconductance, and threshold voltage.[7–13] Similarly, in GaN HEMTs, trapping effects currently place a major limitation on power performance at high frequencies.[8–10] To identify and eliminate the trapping effects in AlGaN/GaN[10–12] and AlInN/GaN[7,14] transistors, a number of studies have been reported in the literature. Surface passivation, as one of these effects, makes it possible to reduce the

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density of surface states, thereby enhancing device performance.[7,9,13,14] Recently, Pozzovivo et al.[7] and Tapajna et al.[14] demonstrated that an Al_2O_3 gate dielectric deposited by metalorganic chemical vapor deposition (MOCVD) strongly reduces excessive gate leakage current compared with the Schottky gate in AlInN/GaN HEMTs. Furthermore, a SiN_x insulator layer has been used successfully for surface state passivation in AlGaN/GaN HEMTs,[10–12] but it has not been used for AlInN/GaN HEMT surface passivation until now.

Capacitance and conductance studies are particularly appropriate for determining the effects of trap states.[15–19] The density of trap states of GaN metal–oxide–semiconductor (MOS) and AlGaN/GaN structures has been evaluated by using frequency-dependent capacitance and conductance measurements.[16,17] Miller et al.[8] and Chu et al.[19] reported on investigations of trap states in AlGaN/GaN heterostructure field-effect transistors (HFETs), and Stoklas et al.[9] reported on a trap density evaluation in AlGaN/GaN MOS heterostructure field-effect transistors (MOSHFETs) by using similar experimental methods.

In the present work, bias-voltage- and frequency-dependent capacitance and conductance measurements were performed on $Al_{0.83}In_{0.17}N$/AlN/GaN and SiN_x/$Al_{0.83}In_{0.17}N$/AlN/GaN heterostructures. Frequency dispersion of admittance was observed, which was analyzed by using an equivalent circuit model. The density and time constant of the surface trap states of both of the samples were calculated. The effects of SiN_x passivation on the surface trap states are discussed herein.

EXPERIMENTAL PROCEDURES

$Al_{1-y}In_yN$/AlN/GaN ($y = 0.17$) heterostructures were grown on c-plane (0001) Al_2O_3 substrates using a low-pressure metalorganic chemical vapor deposition reactor (MOCVD). Prior to epitaxial growth, the Al_2O_3 substrate was annealed at 1100°C for 10 min to remove surface contamination. The growth was initiated with a 15-nm-thick low-temperature (840°C) AlN nucleation layer. Then, a 520-nm high-temperature (HT) AlN buffer layer was grown at a temperature of 1150°C. A 2.100-nm-thick undoped GaN buffer layer (BL) was then grown at 1070°C and at a reactor pressure of 200 mbar. After the deposition of GaN layers, a 2-nm-thick HT-AlN layer was grown at 1085°C at a pressure of 50 mbar. The AlN barrier layer was used to reduce alloy disorder scattering by minimizing wavefunction penetration from the two-dimensional electron gas (2DEG) channel into the AlInN layer.[1] Then, the HT-AlN layer was followed by a 17-nm-thick AlInN ternary layer. This layer was grown at 800°C and a pressure of 50 mbar. Finally, a 3-nm-thick GaN cap layer growth was carried out at a temperature of 1085°C and a pressure of 50 mbar. The In concentration (y) in the $Al_{1-y}In_yN$/AlN/GaN heterostructures was determined by x-ray diffraction (XRD) measurements as $y = 0.17$.

For Hall-effect measurements by the van der Pauw method, square-shaped (5 mm × 5 mm) samples were prepared. Schottky contacts were made as 1.2-mm-diameter circular dots. Prior to ohmic contact formation, the samples were cleaned with acetone in an ultrasonic bath. Then, a sample was treated with boiling isopropyl alcohol for 5 min and rinsed in deionized (DI) water. For ohmic contact formation, Ti/Al/Ni/Au (35 nm/200 nm/50 nm/150 nm) metals were thermally evaporated on the sample and annealed at 750°C for 30 s in N_2 ambient. The measured Hall mobility and sheet carrier concentration, for the unpassivated sample, at room temperature were 820 cm^2/Vs and $4 \times 10^{13}/cm^2$, respectively. After the ohmic contact evaporation, some of the pieces of the $Al_{0.83}In_{0.17}N$/AlN/GaN heterostructure samples were coated with the SiN_x layer by plasma-enhanced chemical vapor deposition (PECVD) with a growth rate of 10 nm/min at 300°C. The refraction index and thickness of the passivation layer were approximately 2.02 and 11.4 nm, respectively, as determined by means of ellipsometry. After the passivation process, the Schottky contacts were formed on both of the samples by Pt/Au (40 nm/70 nm) evaporation.

Current–voltage (I–V) characteristics were measured using a Keithley model 199 dmm/scanner. Capacitance–voltage (C–V) and conductance-voltage (G/ω–V) measurements were performed by using an HP 4192A LF impedance analyzer in the frequency range of 1 kHz to 1 MHz. An alternating-current (AC) signal was attenuated to an amplitude of 40 mV_{rms} to meet the small signal requirement.

RESULTS AND DISCUSSION

Figure 1 compares the current density for the Schottky contact on unpassivated and SiN_x-passivated $Al_{1-y}In_yN$/AlN/GaN heterostructures. As expected, implementation of the SiN_x passivation layer led to significant current reduction in reverse and forward biases. The leakage current density of the SiN_x-passivated heterostructures, at a bias voltage of −4 V, is nearly 28 times lower than that of the unpassivated samples.

Frequency-dependent capacitance and conductance measurements were carried out in a frequency range from 1 kHz to 1 MHz to investigate the trapping effects in the unpassivated and SiN_x-passivated $Al_{1-y}In_yN$/AlN/GaN heterostructures. Figure 2 shows typical experimental C–V characteristics of $Al_{1-y}In_yN$/AlN/GaN heterostructures measured at five different frequencies. Moreover, the experimental C–V curves for the SiN_x/$Al_{1-y}In_yN$/AlN/GaN sample are shown in the inset to Fig. 2. The zero-bias capacitance was approximately 528 nF/cm^2 and 271 nF/cm^2 at 30 kHz for the unpassivated and passivated $Al_{1-y}In_yN$/AlN/

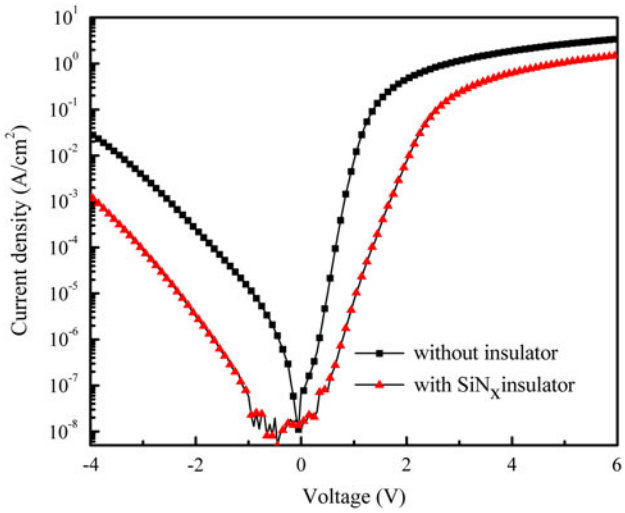

Fig. 1. Measured forward- and reverse-bias current density–voltage characteristics of Schottky contacts on unpassivated and SiN_x-passivated AlInN/AlN/GaN heterostructures.

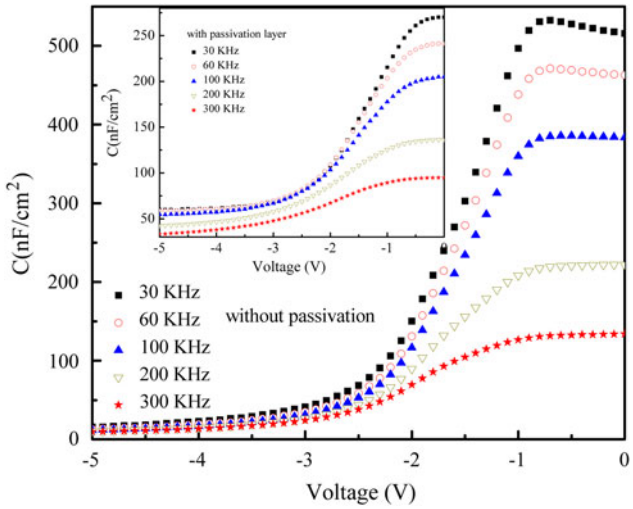

Fig. 2. Measured *C–V* characteristics given for the unpassivated AlInN/AlN/GaN heterostructures for frequencies of 30 kHz, 60 kHz, 100 kHz, 200 kHz, and 300 kHz. The *inset* shows typical *C–V* characteristics for passivated AlInN/AlN/GaN heterostructures.

GaN heterostructures, respectively. The thickness of the AlInN barrier layer $d_{\mathrm{AlInN}} = \varepsilon_r \varepsilon_0 / C_0 \cong 16.4$ nm can be evaluated considering the dielectric constant of the AlInN barrier of $\varepsilon_r = 9.8$ (ε_0 is the vacuum permittivity). The zero-bias capacitance of the metal–insulator–semiconductor (MIS) contact on $Al_{1-y}In_yN$/AlN/GaN is lower than that of the metal–semiconductor (MS) contact on $Al_{1-y}In_yN$/AlN/GaN heterostructures. The thickness of the SiN_x insulator layer (d_{SiN}) was evaluated from the zero-bias MS-to-MIS capacitance ratio, as described by $d_{\mathrm{SiN}} = \frac{\varepsilon_{\mathrm{SiN}} d_{\mathrm{AlInN}}}{\varepsilon_{\mathrm{AlInN}}} \left(\frac{C_{\mathrm{MS}}}{C_{\mathrm{MIS}}} - 1 \right)$. C_{MS} and C_{MIS} are the zero-bias capacitance for the MS and MIS contact on the $Al_{1-y}In_yN$/AlN/GaN heterostructure. $d_{\mathrm{SiN}} \cong 11.1$ nm was obtained as the thickness of the SiN_x layer, which is in good agreement with ellipsometry measurements.

In Fig. 2 and the inset to Fig. 2, the frequency dispersion of the admittance depends strongly on the external bias at low frequency, while the change in capacitance at high frequency becomes very small. In other words, at high frequency, the trap states cannot follow the AC signal and consequently do not contribute appreciably to the capacitance. In the inset to Fig. 2, under a large reverse-bias voltage, the capacitance is small and the corresponding boundary of the depletion layer is in the GaN layer. As the reverse voltage decreases, a capacitance plateau appears, corresponding to depletion of the 2DEG located at the 2DEG channel. Further decrements in the voltage cause a new transition region, wherein the capacitance increases rapidly with decreasing reverse voltage. Moreover, another sharp capacitance slope appears on the right side of the plateau, which indicates that the depletion layer is in the AlInN layer. The surface trap states on the AlInN layer surface cause a deviation between the two curves.

The ohmic to Schottky contact capacitance of an ideal GaN/AlInN/AlN/GaN Schottky diode contains four components: the capacitance of (1) the fully depleted GaN cap layer (C_{GaN}), (2), the AlInN barrier layer (C_{AlInN}), (3) the AlN layer (C_{AlN}), and (4) the GaN depletion region (C_{GaN}). Hereinafter, we consider the AlN layer and AlInN layer as a single layer (because of the small thickness of the AlN layer and lower In concentration in the AlInN layer). The possibility of a lack of compositional uniformity caused by alloy clustering can generate a considerable amount of trap states at the AlInN/AlN/GaN interface (Fig. 3a, b). The electrical behavior of the interface trap states can be modeled using capacitive (C_{it}) and associated resistive terms (R_{it}) for the traps component, in parallel connection with the GaN depletion region capacitor (C_{GaN}). Taking into account the effect of AlInN/AlN/GaN interface trap states, the equivalent circuit of an AlInN/AlN/GaN Schottky diode is modeled as shown in Fig. 3a. In addition to the interface trap states, surface states are present at any metal–semiconductor interface. In general, for Schottky diode fabrication, the semiconductor surface is inevitably covered with a native thin insulating interfacial oxide layer if the semiconductor surface is prepared by the usual polishing and chemical etching process, in which the evaporation of metal is carried out in a conventional vacuum system.[19–22] The interfacial oxide layer is only a few monolayers thick. If this layer's thickness is smaller than 30 Å, most of the states are in equilibrium with the metal.[17,22] This trapping and detrapping process can be modeled as a serial combination of the surface-trap-related resistance (R_{surf}) and capacitance (C_{surf}) in parallel connection with the interfacial oxide layer capacitor (C_{oxide}). With consideration of both the interface and surface trap states, the equivalent

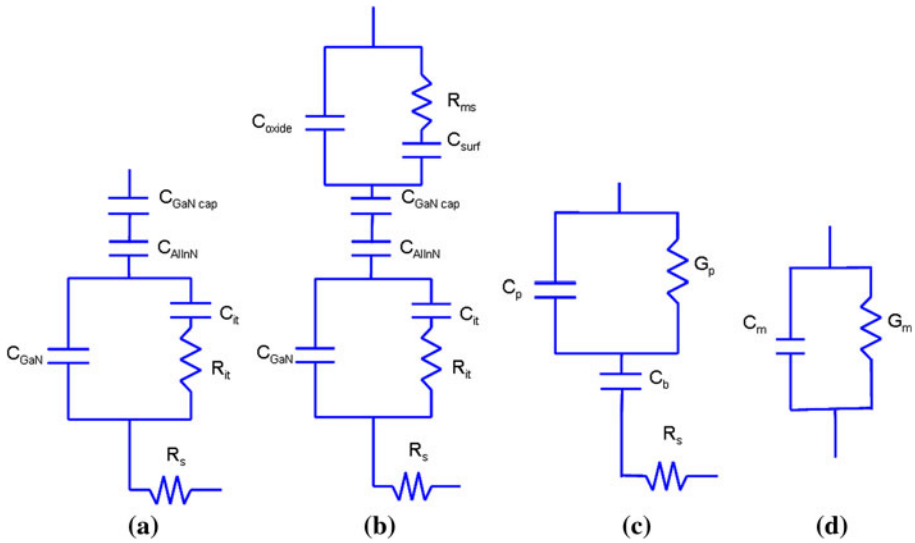

Fig. 3. Equivalent circuit model of Schottky contacts on AlInN/AlN/GaN: (a) with consideration of the interface trap states between the AlInN and GaN layer, (b) considering both the interface and surface trap states, (c) converted to a simplified circuit by considering both the interface and surface trap states, and (d) parameter extraction from the measured circuit.

circuit representation of a GaN/AlInN/AlN/GaN Schottky diode is shown in Fig. 3b. Furthermore, in addition to the interface and surface trap states, there may also be traps that are related to crystal defects and imperfections within the bulk GaN and AlInN layers. However, the bulk states have time constants as long as milliseconds, making their effects unobservable by admittance and current–voltage measurement methods.[8,9,19,23] These traps states can be detected by using the deep-level transient spectroscopy (DLTS) method.[24] For these reasons, the bulk states were not considered in this analysis.

In Fig. 2, the frequency dispersion of the admittance strongly depends on the external bias, and states can be eliminated, and the effect of the surface trap states can be extracted by comparing the measured admittance values at the deep accumulation and weak depletion regime.

As shown in Fig. 3d, the capacitance and conductance of the Schottky diode were measured simultaneously, assuming a parallel combination of C_m and G_m. The method described by Schroder for the interface trap states in a metal–oxide–silicon system was used in these studies for the analysis of AlInN/AlN/GaN heterostructures with care given to the surface traps.[8,9,16,17,19,23,25]

The parallel capacitance C_p and conductance G_p/ω can be obtained from measured C_m and G_m/ω curves by using the relation[8,17]

$$C_p = \frac{-C_b[(C_m^2 - C_m C_b)\omega^2 + G_m^2]}{\omega^4 C_m^2 C_b^2 R_s^2 + \omega^2(C_b^2 R_s^2 G_m^2 + C_m^2 + C_b^2 - 2C_b^2 R_s G_m - 2C_m C_b) + G_m^2}, \quad (1a)$$

$$\frac{G_p}{\omega} = \frac{-\omega C_b^2(R_s C_m^2 \omega^2 + R_s G_m^2 - G_m)}{\omega^4 C_m^2 C_b^2 R_s^2 + \omega^2(C_b^2 R_s^2 G_m^2 + C_m^2 + C_b^2 - 2C_b^2 R_s G_m - 2C_m C_b) + G_m^2}. \quad (1b)$$

becomes significant in the deep accumulation regime (at zero or near very small reverse voltage), in turn indicating that surface trap states are the dominant trapping mechanism in the 10 kHz to 1 MHz frequency range.[8,19] Because of these reasons, the component related to the interface trap

In the equation, we take the barrier capacitance C_b as the total of the C_{AlInN} and $C_{GaN\ cap}$ capacitance values. C_b was determined from the plateau in the C–V curve associated with the accumulation of electrons in the two-dimensional electron gas channel. R_s is the series resistance of the ohmic

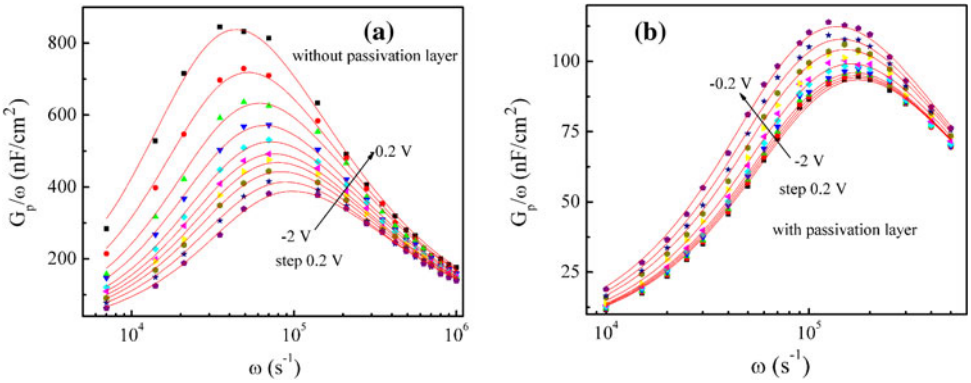

Fig. 4. Parallel conductance as a function of frequency for AlInN/AlN/GaN heterostructures: (a) without passivation and (b) with a SiN_x passivation layer, at different bias voltages. The *solid curves* are the best fits of Eq. 2b to the experimental data.

contact. The R_s values near the origin were evaluated using a method developed by Cheung and Cheung.[26]

By plotting C_p and G_p/ω as functions of frequency and by fitting the resulting curves to the equations derived by AC analysis, the surface trap density D_{st} and trap state time constant τ_{st} can be extracted. The equivalent parallel capacitance C_p and conductance G_p/ω as functions of frequency, assuming a continuum of trap levels, can be expressed as[8,9,16,17,23,25]

$$C_p = C_{oxide} + \frac{qD_{st}}{\omega\tau_{st}\tan(\omega\tau_{st})}, \tag{2a}$$

$$\frac{G_p}{\omega} = \frac{qD_{st}}{2\omega\tau_{st}}\ln\left[1+\omega^2\tau_{st}^2\right]. \tag{2b}$$

Figure 4 shows the calculated G_p/ω versus $\ln(\omega)$ curves of the $Al_{1-y}In_yN$/AlN/GaN and SiN_x/$Al_{1-y}In_yN$/AlN/GaN heterostructures for different bias voltages. G_p/ω versus $\ln(\omega)$ gives a peak for each bias voltage value due to the D_{st} contribution. It can be clearly seen that the peak amplitude of G_p/ω increases and the peak position shifts to lower frequency values, when the bias voltage is varied from negative values to zero. D_{st} and τ_{st} were calculated by fitting Eq. 2b to the experimental G_p/ω versus $\ln(\omega)$ curves.

Figure 5 shows the extracted D_{st} and τ_{st} values as a function of energy separation from the conduction-band edge. The resulting calculated parameters of the unpassivated $Al_{1-y}In_yN$/AlN/GaN were $D_{st} \cong (4-13)\times 10^{12}$ eV^{-1} cm^{-2} and $\tau_{st} \approx 3$ μs to 7 μs for the surface trap states, respectively. For the passivated sample, the surface states density D_t decreased to $D_{st} \cong 1.5\times 10^{12}$ eV^{-1}cm^{-2} and the time constant to $\tau_{st} \approx 1.8$ μs to 2 μs. The density of the surface traps in the passivated $Al_{1-y}In_yN$/AlN/GaN heterostructures is nearly one order of magnitude lower than that in the unpassivated $Al_{1-y}In_yN$/AlN/GaN heterostructures. This shows that the $Al_{1-y}In_yN$ surface was successfully passivated by the SiN_x layer. The SiN_x passivation process

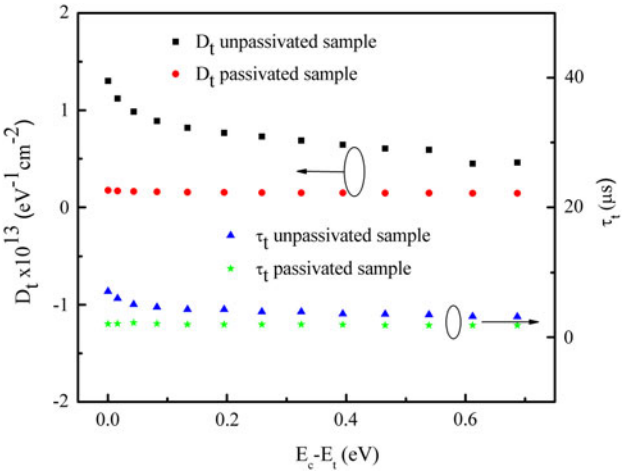

Fig. 5. Experimentally derived trap states density (D_{st}) and time constants (τ_{st}) for interface states as a function of $E_c - E_t$ for unpassivated and passivated AlInN/AlN/GaN heterostructures.

is more effective for the surface traps, which are located near the conduction-band edge.

The trap states in the $Al_{1-y}In_yN$/AlN/GaN heterostructures may be located at the AlInN surface, in the AlInN barrier layer, at the AlInN/AlN/GaN heterointerface, or in the GaN buffer layer.[8,9,19] The trap states within the AlInN and GaN layers are usually deep below the conduction-band edge and have time constants as long as milliseconds, in which case their effects are not observable in the 10 kHz to 1 MHz frequency range.[8,19] Miller et al.[8] used various models to determine the exact location of the trap states at the heterojunction, in the bulk of the barrier layer, and at the metal–semiconductor interface. However, the location of the traps could not be determined unambiguously. Stoklass et al.[9] revealed two different types of trap states, slow (8 ms) and fast (0.1 μs to 1 μs), in AlGaN/GaN (HFETs) as well as MOSHFETs. They attributed the slow traps to surface states and assumed that the fast traps were related to bulk states. However, we attribute the measured trap states in $Al_{1-y}In_yN$/AlN/GaN heterostructures as surface states.

The external bias-dependent frequency dispersion in the deep accumulation regime (at zero or near very small reverse voltage) indicates that the surface trap states are the dominant trapping mechanism in $Al_{1-y}In_yN/AlN/GaN$ and $SiN_x/Al_{1-y}In_yN/AlN/GaN$ heterostructures.

CONCLUSIONS

To investigate the trapping effects in $Al_{0.83}In_{0.17}N/AlN/GaN$ and $SiN_x/Al_{0.83}In_{0.17}N/AlN/GaN$ heterostructures, frequency-dependent capacitance and conductance analysis were performed using an equivalent circuit model. The density (D_t) and time constant (τ_t) of the surface trap states have been determined as a function of energy separation from the conduction-band edge ($E_c - E_t$). The D_{st} and τ_{st} values of the surface trap states for unpassivated samples were found to be $D_{st} \cong (4-13) \times 10^{12}$ eV^{-1} cm^{-2} and $\tau_{st} \approx 3$ μs to 7 μs, respectively. For the passivated sample, the D_{st} values decreased to 1.5×10^{12} $eV^{-1}cm^{-2}$ and the τ_{st} values decreased to 1.8 to 2 μs. The surface trap states density in $Al_{0.83}In_{0.17}N/AlN/GaN$ heterostructures decreased by approximately one order with SiN_x passivation. These indicate that the SiN_x insulator layer between the metal contact and the surface of the $Al_{0.83}In_{0.17}N$ layer can passivate surface states effectively.

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