Research Article

SURFACE and INTERFACE ANALYSIS

Received: 26 August 2009 Revised: 2 December 2009 Accepted: 11 January 2010 Published online in Wiley Interscience: 28 March 2010

(www.interscience.wiley.com) DOI 10.1002/sia.3248

The effect of insulator layer thickness on the main electrical parameters in *(Ni/Au)*/$Al_xGa_{1-x}N$/AlN/GaN heterostructures†

Şemsettin Altındal,[a]* Yasemin Şafak,[a] İlke Taşçıoğlu[a] and Ekmel Özbay[b]

(Ni/Au)$Al_xGa_{1-x}N$/AlN/GaN($x = 0.22$) heterostructures with and without a passivation layer of the SiN_x were fabricated in order to see the effect of the insulator layer on the main electrical parameters such as zero-bias barrier height (BH) (Φ_{B0}), ideality factor (n), series resistance (R_s) of the structure, and the interface state density (N_{ss}). Some of these parameters were determined from both $I-V$ and admittance ($C-V$ and $G/\omega-V$) measurements at room temperature and at 1 MHz and were compared. The experimental results show that the value of N_{ss} in a Schottky contact without passivation is nearly 1 order of magnitude larger than that in a Schottky contact with SiN_x passivation layers. Also, the values of R_s increase with the increasing thickness of the passivation layer. In the forward bias region, the negative values of capacitance are an attractive result of this study. This negative capacitance disappears in presence of the passivation layer. Copyright © 2010 John Wiley & Sons, Ltd.

Keywords: (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN heterostructures; interface states; negative capacitance; frequency dependence; series resistance

Introduction

When the thickness of SiO_2 is less than 20 Å, it will have unacceptably large leakage current due to the direct tunneling mechanism and low dielectric constant. A poor interface of the insulator/oxide film with Si also leads to high leakage current, high-temperature dispersion, and high defect trapped charges. Therefore, the fundamental requirements for the materials are high dielectric constant, low density of interface states, and low leakage current.[1–9] In recent years high dielectric materials have been proposed for application as an insulator layer at the metal/semiconductor (M/S) interface such as a metal–TiO_2–semiconductor (MIS or MOS), metal–$Bi_3Ti_4O_{12}$–semiconductor (MFS) structures, and high electron mobility transistors (HEMTs).[10]

In addition, there are various nonidealities in these structures, such as the formation of an insulator layer at the M/S interface, the energy distribution profile of N_{ss} at the semiconductor/insulator (S/I) interface, R_s, and inhomogeneous barrier heights (BHs). The values of N_{ss} and R_s of these devices are important parameters that affect both $I-V$ and $C-V$ characteristics.[1,3,11,12] In general, the forward bias $I-V$ characteristics are linear in the semilogarithmic scale at intermediate bias voltages (~0.1–0.8 V), but deviate from the linearity due to the effect of R_s and interfacial layer.[3,11,12] Since a bias voltage is applied across these structures, the combination of the interfacial insulator layer, depletion layer, and series resistance of the device will share the applied bias voltage. In recent years, some studies[1,3,4,11] investigated the effect of existence of an interfacial insulator/oxide layer and the N_{ss} on the behavior of Schottky barrier diodes (SBDs), and extracted the N_{ss} from the forward bias $I-V$ characteristics.

The main aim of this study is to investigate the effect of the passivation layer on some of the main electrical parameters of (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN($x = 0.22$) heterostructures by using $I-V$, $C-V$, and $G/\omega-V$ measurements at room temperature. The values of R_s were determined from both Cheung's[13] and conductance[14] methods. In addition, the N_{ss} profile was obtained from both the forward bias $I-V$ characteristics by taking into account the bias dependence of the effective BH (Φ_e) and low-high frequency $C-V$ characteristics.

Experimental

The (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN($x = 0.22$) heterostructures were fabricated on c-plane (0001) double-polished Al_2O_3 substrates of 2-inch diameter in a low pressure metal-organic chemical vapor deposition (MOCVD). Al_2O_3 substrate was annealed at 1100 °C for 10 min in order to remove surface contamination. The buffer structures consisted of a 15-nm-thick, low-temperature (650 °C) AlN nucleation layer, and high-temperature (1150 °C) 420-nm AlN templates. A 1.5-μm nominally undoped GaN layer was grown on an AlN template layer at 1050 °C, followed by a 2-nm-thick high-temperature AlN (1150 °C) barrier layer. The ohmic contacts were formed as a square van de Pauw shape and the Schottky contacts formed as 1-mm-diameter circular dots. Then, Schottky contacts were formed by Ni/Au (40/80 nm) evaporation. The schematic diagram of (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN ($x = 0.22$) heterostructures can be seen in our previous study.[10] After the formation of the ohmic contact, the SiN_x layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) on

* *Correspondence to: Şemsettin Altındal, Department of Physics, Gazi University, 06500 Ankara, Turkey. E-mail: altundal@gazi.edu.tr*

† *Paper published as part of the ECASIA 2009 special issue.*

a *Department of Physics, Gazi University, 06500 Ankara, Turkey*

b *Nanotechnology Research Center, Department of Physics, Bilkent University, 06800 Ankara, Turkey*

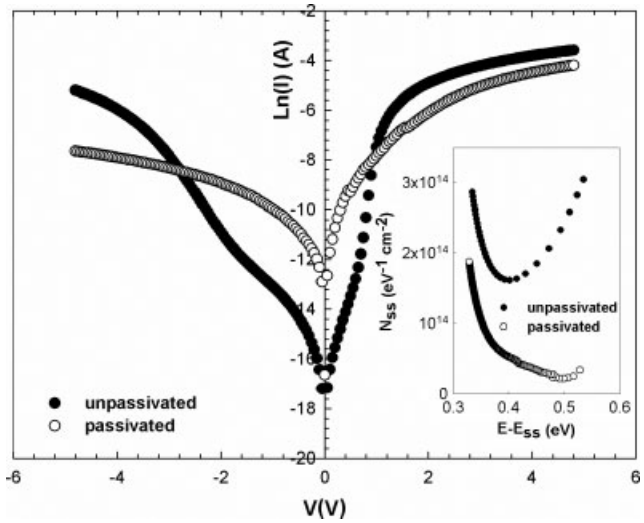

Figure 1. (a) Forward and reverse bias *I–V* characteristics and (b) energy distribution profile of N_{ss} obtained from forward bias *I–V* data for two samples at room temperature.

(Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN ($x = 0.22$) heterostructures at 300 °C. The thickness of SiN_x was about 100 Å for passivated sample, which was predicted from the growth time. The *I–V* and admittance (*C–V* and G/ω–*V*) measurements of the (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN ($x = 0.22$) heterostructures were taken using a computer controlled Keithley 2400 Sourcemeter and an HP4192 A LF impedance analyzer at room temperature.

Results and Discussions

Forward bias *I – V* characteristics

The forward bias semilogarithmic *I–V* characteristics of the (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN($x = 0.22$) heterostructures with and without SiN_x passivation layer are given in Fig. 1. According to the thermionic emission (TE) theory, the relationship between the applied bias and the current through a barrier is given by Sze[11] and Rhoderick and Williams[12]

$$I = \underbrace{AA^*T^2 \exp\left(-\frac{qB0_\Phi}{kT}\right)}_{I_0} \exp\left(\frac{q(V - IR_s)}{nkT}\right) \left[1 - \exp\left(\frac{-q(V - IR_s)}{nkT}\right)\right] \quad (1)$$

where Φ_{B0} is the zero-bias BH, *A* is the rectifier contact area, A^* is the effective Richardson constant and is equal to 32.09 A/cm^2 K^2 for undoped $Al_{0,22}In_{0,78}N$,[10] in which I_0 is the reverse saturation current derived from the straight line intercept of ln*I* at zero-bias voltage.[11] The voltage drop across the series resistance of the diode is $V_d = V - IR_s$. In Eqn (1), *n* is the ideality factor, *T* is the absolute temperature in Kelvin, *k* is the Boltzmann constant, and *V* is the applied voltage across the structure. The values of Φ_{B0} and *n* are obtained from the following equations,[11,12] respectively:

$$\Phi_{B0} = \frac{kT}{q} \ln\left(\frac{AA^*T^2}{I_0}\right) \quad (2a)$$

$$n = \left(\frac{dV}{d\ \ln(I)}\right)\frac{q}{kT} \quad (2b)$$

The values of Φ_{B0} and *n* were found to be as 0.61 eV and 4.99 and 0.54 eV and 7.09, for unpassivated and passivated samples, respectively. The high values of the ideality factor of these structures can be explained by means of the effects of the bias voltage drop across the insulator layer, surface states, bias dependence of the BH, and barrier inhomogeneity at the M/S interface.[1,11,12] As can be seen in Fig. 1, the downward curvature at sufficiently high bias voltages was caused by the effect of R_s, apart from the existence of the interface states.[3,9–13] Therefore, the values of *n*, BH, and R_s were evaluated by using a method that was developed by Cheung and Cheung[13] in the high bias voltage range as in following equations:

$$\frac{dV}{d(\ln I)} = n\frac{kT}{q} + IR_s \quad (3a)$$

$$H(I) = V - n\frac{kT}{q}\ln\left(\frac{I}{AA^*T^2}\right) = IR_s + n\Phi_b \quad (3b)$$

where Φ_b is the BH obtained from the data of the downward curvature region in the forward bias *I–V* characteristic. Figure 2(a) and (b) shows the experimental $dV/d(\ln I)$ vs *I* and *H*(*I*) vs *I* plots for two samples and both the plots give straight lines. Furthermore, from Eqn (3a) and (3b) the main values of R_s were found to be 130.58 and 179.21 Ω for unpassivated and passivated samples, respectively.

The energy distribution profile of N_{ss} was obtained from forward bias *I–V* data using the following equations and is given in the inset of Fig 1.

$$\Phi_c = \Phi_{B0} + \beta V = \Phi_{B0} + \left(\frac{d\Phi_e}{dV}\right)V = \Phi_{B0} + \left(1 - \frac{1}{n(V)}\right) \quad (4)$$

where $d\Phi_e/dV$ is the change in the barrier with bias voltage, β is the voltage coefficient of the effective BH (Φ_e). As proposed by Ref. [1], the voltage dependent *n* is given by

$$n = \frac{q}{kT}\frac{dV}{d\ \ln I} = \frac{I}{(1 - d\Phi_{B0}/dV)} \quad (5)$$

and the expression for the density of the N_{ss} is reduced as

$$N_{ss} = \frac{1}{q}\left[\frac{\varepsilon_i}{\delta}(n-1) - \frac{\varepsilon_s}{W_D}\right] \quad (6)$$

where δ is the thickness of the passivation layer, W_D is the depletion layer width that is being deduced from the experimental *C–V* measurements at 1 MHz, and ε_i and ε_s are the permittivity insulator layer and semiconductor, respectively. As can be seen in the inset of Fig. 1, for two samples there was a slight exponential increase in N_{ss} from the midgap toward the bottom of the conductance band, but in the case of the unpassivated sample the distribution profile of N_{ss} was similar to the U shape. Also, the experimental results show that the value of N_{ss} in the unpassivated heterostructure is nearly 1 order of magnitude larger than the passivated heterostructure.

Forward and reverse bias *C – V* and *G*/ω characteristics

Figure 3(a) and (b) shows the *C–V* measurements at low (5 kHz) and high (1 MHz) frequencies for both unpassivated and passivated (Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN($x = 0.22$) heterostructures, respectively. At sufficiently high frequencies ($f \geq 1$ MHz), the charges at interface cannot follow the a.c. signal, because in this

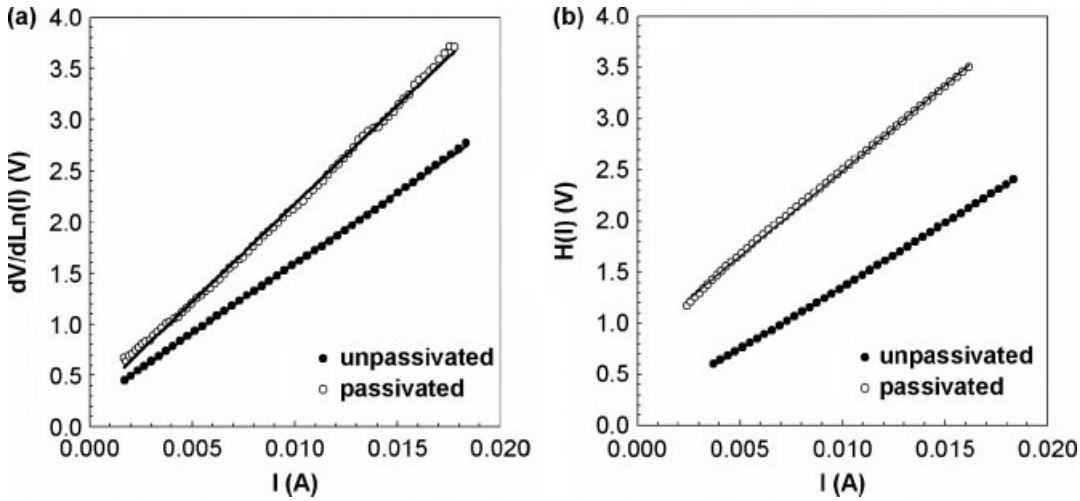

Figure 2. (a) $dV/d\ln(I) - I$ and (b) $H(I) - I$ characteristics for two samples at room temperature.

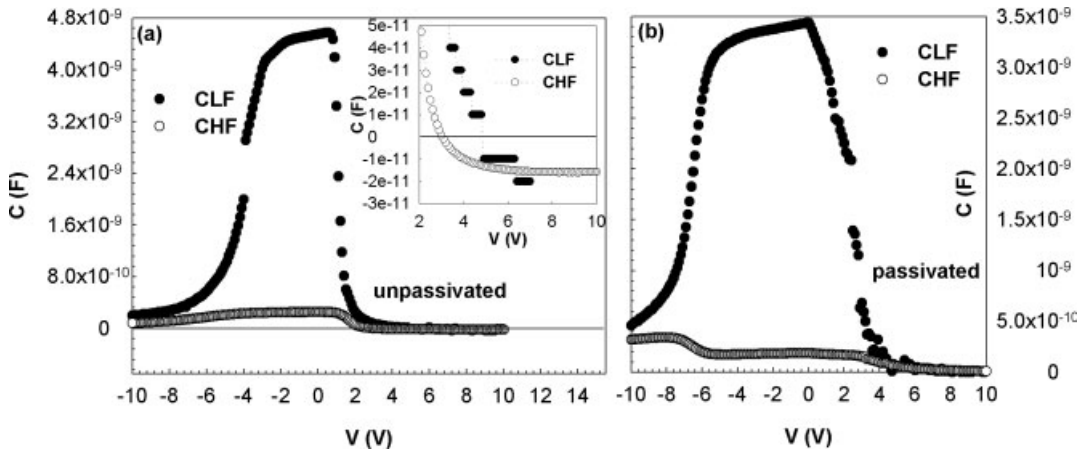

Figure 3. (a) and (b) $C-V$ characteristics for two samples at room temperature and at low (5 kHz) and high (1 MHz) frequencies.

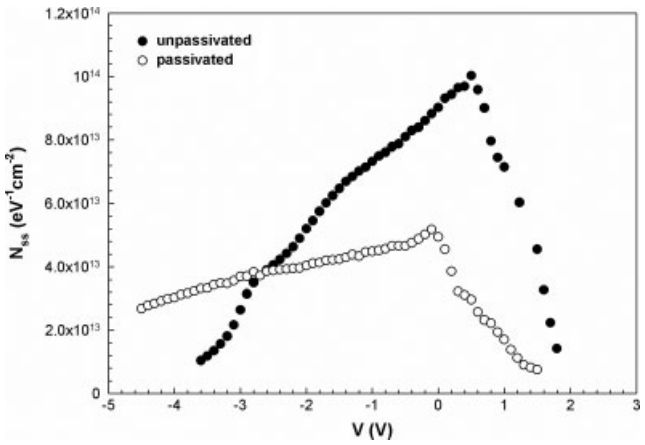

Figure 4. The density distribution profile of N_{ss} for two samples, obtained from the low-high frequency capacitance ($C_{LF} - C_{HF}$) method at room temperature.

frequency the carrier life time of charge (τ) become larger than the measured period.[11,14] The $G/\omega - V$ characteristics were also obtained in this study but are not given here. They did not show a negative behavior. As can be seen in the inset of Fig. 3(a), the most interesting behavior of the forward bias $C-V$ characteristics for unpassivated sample is the negative capacitance at high bias voltage regions as well as on many electronic devices, which has been reported in the literature.[15–17] Contrary to the unpassivated sample, the passivated one's $C-V$ plots did not show a negative capacitance behavior. In this work, we have considered that the interfacial material (SiN_x) can reduce the magnitude of N_{ss} and prevent negative capacitance. Jones *et al.*[18] show that the negative capacitance caused by the injection of minority carriers can only be observed at a forward applied bias voltage.

The structures of many electronic devices such as MIS, MFS or MFIS, and HEMT consist the N_{ss} and bulk traps where the charges can be stored and released when the appropriate forward applied bias and the external (a.c.) oscillation voltage are applied, in which a large effect can be produced on the devices.[16,18]

The density distribution profile of N_{ss} for both unpassivated and passivated samples was also obtained from the low-high frequency capacitance ($C_{LF} - C_{HF}$) measurements by using following Eq. [7] and given in Fig. 4.[14]

$$N_{ss} = \frac{1}{qA}\left[\left(\frac{1}{C_{LF}} - \frac{1}{C_i}\right)^{-1} - \left(\frac{1}{C_{LF}} - \frac{1}{C_i}\right)^{-1}\right] \quad (7)$$

where C_{LF} and C_{HF} are the measured low frequency capacitance (5 kHz) and high frequency capacitance (1 MHz), respectively, and C_i is the insulator layer capacitance. As can be seen in Fig. 4, the values of N_{ss} decrease with an increase of the passivation layer thickness, which is in agreement with the N_{ss} values that were obtained from the forward bias I–V measurements.

Conclusions

(Ni/Au)/$Al_xGa_{1-x}N$/AlN/GaN($x = 0.22$) heterostructures with and without a passivation layer of the SiN_x were fabricated in order to see the effect of the interfacial layer and N_{ss} on the main electrical parameters at room temperature. The density distribution profiles of N_{ss} were obtained from both I–V and the low-high frequency capacitance (C_{LF}–C_{HF}) methods. Both the experimental methods show that the value of N_{ss} in a Schottky contact without passivation is nearly 1 order of magnitude larger than the Schottky contact with SiN_x passivation layers. Also, the values of R_s were obtained by using Cheung's functions from the forward bias I–V characteristics and they increase with the increasing thickness of the passivation layer. The interesting result in this study is the observation of the negative capacitance in the unpassivated sample. In contrast to the passivated sample, in the forward bias region the value of C for unpassivated sample shows a negative behavior. As a result, we can say that the interfacial material (SiN_x) can both reduce both the magnitude of N_{ss} and prevent negative capacitance.

References

[1] H. C. Card, E. H. Rhoderick, *J. Phys. D: Appl. Phys.* **1971**, *4*, 1589.
[2] Y. Dökme, *Physica B* **2007**, *388*, 10.
[3] O. Pakma, N. Serin, T. Serin, Ş. Altindal, *J. Sol-Gel Sci. Tech.* **2009**, *50*(1), 28.
[4] M. K. Hudait, S. B. Krupanidhi, *Solid State Electron.* **2000**, *44*, 1089.
[5] T. Hashizume, S. Ootomo, H. Hasegawa, *Phys. Stat. Solidi C* **2003**, 2380.
[6] M. K. Bera, S. Chakraborty, S. Saha, D. Paramanik, S. Varma, S. Bhattacharya, C. K. Maiti, *Thin Solid Films* **2006**, *504*, 183.
[7] S. Zeyrek, Ş. Altindal, H. Yüzer, M. M. Bülbül, *Appl. Surf. Sci.* **2006**, *252*, 2999.
[8] C. Y. Liu, T. Y. Tseng, *Ceramics Int.* **2004**, *30*, 1101.
[9] F. Parlaktürk, Ş. Altindal, A. Tatarodlu, M. Parlak, A. Agasiyev, *Microelectron. Eng.* **2008**, *85*, 81.
[10] E. Arslan, Ş. Altindal, S. Ozcelik, E. Ozbay, *J. Appl. Phys.* **2009**, *105*, 023705.
[11] S. M. Sze, *Physics Semiconductor Devices*, John Wiley & Sons: New York, **1981**.
[12] E. H. Rhoderick, R. H. Williams, *Metal Semiconductor Contacts* (2nd edn), Clarendon Press: Oxford, **1988**.
[13] S. K. Cheung, N. W. Cheung, *Appl Phys. Lett.* **1986**, *49*, 85.
[14] E. H. Nicollian, J. R. Brews, *MOS (Metal Oxide Semiconductor) Physics and Technology*, Wiley: New York, **1982**.
[15] R. Gharbi, M. Abdelkrim, M. Fathllah, E. Tresso, S. Ferrero, C. F. Piri, T. Mohamed Brahim, *Solid State. Electron.* **2006**, *50*, 367.
[16] J. Bisquert, G. Garcia-Belmonte, A. Pitarch, H. J. Bolink, *Phys. Lett.* **2006**, *422*, 184.
[17] X. Wu, E. S. Yang, H. L. Evans, *J. Appl. Phys.* **1990**, *68*, 2845.
[18] B. K. Jones, J. Santana, M. McPherson, *Solid State Commun.* **1988**, *107*, 47.