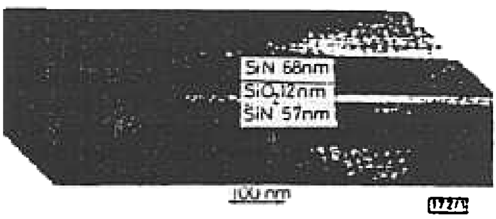
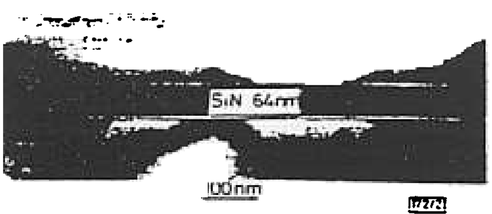
ilm of silicon dioxide is formed on the nitride layer during a ›re-bonding oxidation.[5]

:xperiment: Wafers with hydrophobic silicon nitride on both ides were oxidised in wet oxygen at 1100°C for two hours. \fter the oxidation process the wafers were found to be ıydrophilic. After cleaning and hydration in a hot peroxide olution the wafers were rinsed and dried in a spin dryer, then ›rought into intimate contact where initial bonding occurred. 'he initial bonding was performed for silicon nitride to silicon ›itride and silicon nitride to hydrophilic silicon wafers. The vafers with LPCVD nitride whose surfaces were hydrophilic vithout preoxidation were directly bonded between nitride-›itride and nitride-silicon. Following the initial bonding the vafer pairs were annealed at 1000°C in dry O_2 for one hour. 'he wafers remained solidly bonded during and after the nneal. Attempts to physically separate the wafers resulted in ›reaking of the wafers.

lesults and discussions: Silicon nitride was successfully onded to silicon nitride and silicon without using any adhe-ive. The naturally hydrophilic silicon nitrides bonded readily fter thermal oxidation. We found wafers of LPCVD silicon itride that are naturally hydrophilic direct bond readily vithout an oxidation treatment. Figs. 1 and 2 show TEM ıicrographs of the cleaved interface of silicon nitride-silicon itride and silicon nitride-silicon bonded wafer pairs, respec-vely. The nitride wafers in Fig. 1 were initially hydrophobic, ut became hydrophillic after a steam oxidation. This 12 nm ıermal oxide between the silicon nitrides is clearly seen in the ıicrograph. The nitride wafer in Fig. 2 was initially hydro-hillic, and no thermal oxidation was performed on either 'afer prior to the bonding.



ig. 1 *TEM micrograph of silicon nitride coated silicon wafers*



g. 2 *TEM micrograph of a silicon nitride coated silicon wafer which ıs been bonded to a silicon wafer*

onclusions: In summary, this letter has described the tech-ques for applying silicon fusion bonding to nitride coated afers. We have established the need for the bonding surface be hydrophillic and have achieved this by the deposition or oxidation of the deposited layer. Since silicon nitride is ›mmonly used for its electrical isolation, contamination sistance and extreme hardness, this technique should be a ry useful addition to devices made using silicon bonding.

:knowledgments: The authors wish to thank Hughes Aircraft ›mpany for supplying materials and support for this work.

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18th April 1990

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PULSE FORMING AND TRIGGERING USING RESONANT TUNNELLING DIODE STRUCTURES

Indexing terms: Semiconductor devices and materials, Resonance, Tunnel diodes, Pulse generation

Resonant tunnelling diodes (RTDs) monolithically integrated with coplanar transmission lines have been used for pulse formation, with measured rise times as low as 6 ps. Triggering at 60 GHz was performed by using the RTD pulser structures as trigger circuits.

Introduction: Resonant tunnelling diodes (RTDs) have been the subjct of intensive research since Sollner *et al.* demonstrated the high frequency characteristics of these devices.[1] In a recent letter, we investigated the switching performances of RTD's.[2] Using a simple circuit model, it was shown that the switching times of RTDs are not limited by quantum mechanical time constants, but by the RC time constants of the device. That work emphasised the importance of minimising device capacitance and maximising peak current density, while keeping a reasonable peak to valley ratio. Following this approach, we have fabricated high current density, microwave compatible RTDs.[3]

In this letter, we report the use of RTD structures for two switching applications: as pulse generators with as low as 6 ps rise times and as trigger circuits operating up to 60 GHz. Our circuits outperformed both the Esaki tunnel diode pulse generator circuits and Esaki tunnel diode trigger circuits by a factor of three in speed.

Experiment: The pulse forming structure consists of a 50 Ω coplanar transmission line with a RTD shunted to ground from the conductor centre of the line.[2] Switching was demonstrated by applying a DC bias and a 1·24 GHz sine wave to the transmission line. In order to see repeating switching waveforms, the amplitude of the sine wave must be large enough to first switch the load line above the peak voltage of the RTD and then move the load line back down below the valley voltage to reset the device. Fig. 1 illustrates the expected output waveform corresponding to such a sinusoidal input voltage. For devices tested with applied sinusoidal voltages, the switching transition was typically less than 70% of the total output voltage swing.

As the RTD switches, a step waveform begins to propagate along the transmission line. The resulting waveform can be measured by electro-optically sampling the voltage at a point just past the device.[4] The length of the transmission line was chosen to be long enough to allow measurement of the pulse risetime before any reflections return from the output pad. This allows us to see the actual switching of the device, independent of bond pad capacitance. Electronic probing techniques, by contrast, will be limited by the bond pad capacitance rather than by the device characteristics. The effects of bond pad capacitance in electronic measurements can be minimised by making larger area devices with device capacitances much larger than the bond capacitance. However, it is difficult to satisfy the optimum load conditions with larger area devices. A typical electro-optically sampled pulse is shown in Fig. 2. 10–90% switching transition times as low as 6 ps were measured with voltage swings of 400–500 mV. This is a factor of three improvement over Esaki tunnel diode pulse generators which have 20 ps minimum rise times.

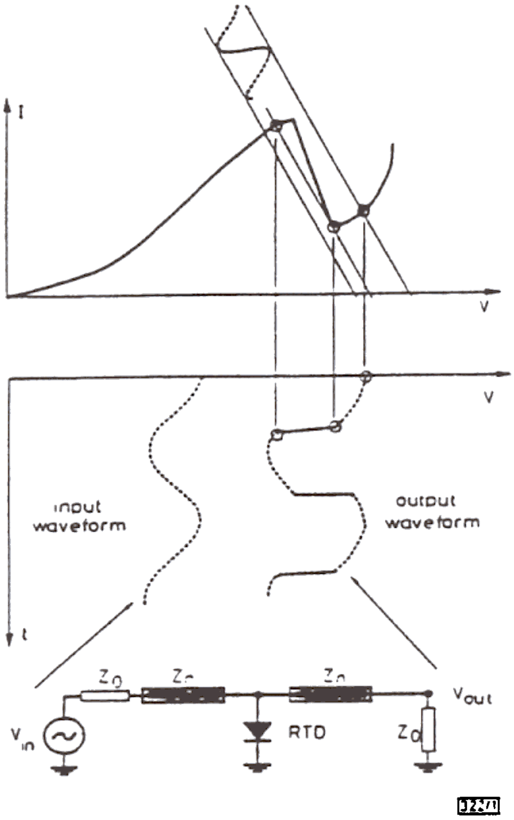


Fig. 1 *Expected waveform when the pulse forming structure is driven by a sinusoidal input*

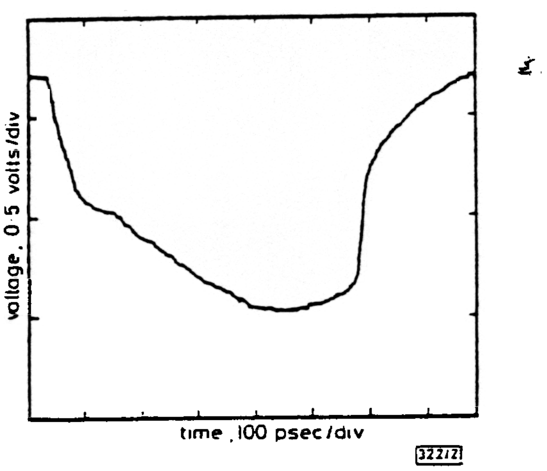


Fig. 2 *Electro-optically sampled output waveform of the pulse forming structure*

Triggering is one application in which resonant tunnelling diodes can lead to improved performances over Esaki tunnel diodes. The principles of trigger circuits have been explained elsewhere.[5] The device used as a threshold detector must have two threshold levels and hysteresis. The hysteresis, which differentiates this circuit from a limiter in which the output is continuous, eliminates the output fluctuations caused by noise when the input reaches the threshold level. This type of circuit can be realised in two ways: as a Schmitt trigger using transistors, or as a trigger circuit using Esaki tunnel diodes. In terms of speed, Esaki tunnel diode trigger circuits are superior to Schmitt triggers; 20 GHz Esaki tunnel diode trigger circuits have been introduced commercially whereas Schmitt triggers are used for lower frequency applications.

Triggering is similar to the pulse forming described, but now a DC bias and the sum of two different signals are applied to the transmission line. One signal is a high frequency (HF) sinusoid with a relatively small amplitude. The other signal is a relatively slow sinusoid with a larger amplitude. The resulting sum resembles an HF signal superimposed on a slowly rising ramp function. For such an input voltage, switching occurs near the maximum of the HF signal. The train of switching pulses generated on the transmission line is then synchronous with the HF signal and can be used for triggering in other experiments. To check that the pulse trains are synchronous with the HF signal, the DC bias is changed by small increments. If the pulses are synchronous, then at certain bias levels the device switching shifts to the next peak of the HF signal. The time delay between the new pulse obtained with the new bias and that obtained with the previous bias increases by one period of the HF signal.

Equipment: To test this principle at 40 GHz, we use the following experimental set-up: A large amplitude, 500 MHz sinusoid from a frequency synthetiser, is fed into a power splitter. One output of the splitter triggers the oscilloscope. The other is summed with a relatively small amplitude 40 GHz signal from another phase-locked synthetiser and used to drive the device through a transmission line. The DC bias is increased in 12 mV steps and each time a different switching waveform is recorded (Fig. 3). The first two (A, B)

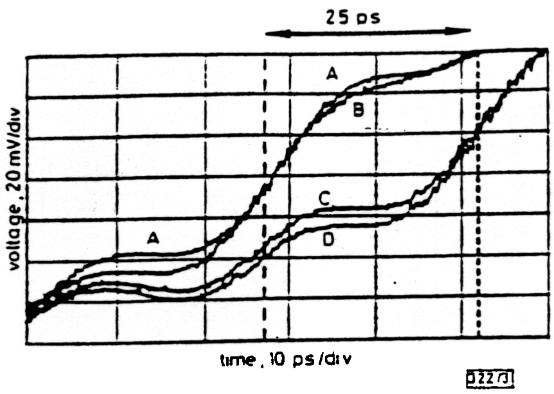


Fig. 3 *Four different switching waveforms are obtained by changing the DC bias in 12 mV steps*

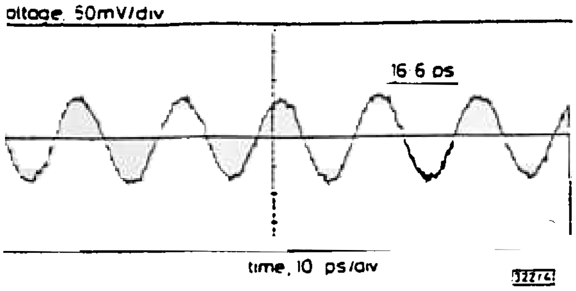
The time delay between the waveforms A, B and C, D approximately 25 ps, equal to one period of 40 GHz signal

waveforms correspond to switching around one of the maxima of the 40 GHz signal. Although bias is changed by 12 mV between A and B, there is no change in time delay between A and B. But another 12 mV bias change between B and C results in a sudden increase of approximately 25 ps (one period of the 40 GHz signal) in delay between B and C. This shows that the switching waveform is synchronous with the 40 GHz signal.

To demonstrate useful triggering, the output of the RTD circuit is applied to the trigger input of a HP 54124 digitising oscilloscope. This time a 60 GHz signal is fed into a power splitter. One output of the splitter is fed to the input of the oscilloscope. The other is summed with a relatively large amplitude slow signal and applied to the device through the transmission line. To ensure that the triggering is not due to the synchronisation of the slow signal with the 60 GHz signal, a 499 MHz slow signal is chosen. Observation of the 60 GHz signal is shown in Fig. 4, which demonstrates triggering of a 60 GHz signal using the RTD circuit. This is at a frequency three times higher than obtained with conventional trigger circuits using Esaki tunnel diodes.

Conclusion: In summary, we have demonstrated 6 ps switching time and triggering at 60 GHz using RTDs. We believe that the operating frequency of our triggering experiment result is limited by the experimental setup, not the device itself, and it can be further increased to the 100 GHz region.

nowledgment: The authors are grateful to M. J. W. dwell, A. Black and M. Shakouri for their valuable help in



. 4 Oscilloscope trace of a 60 GHz signal triggered by the output of RTD circuit

: high frequency measurements, Y. C. Pao for the material wth, and B. A. Auld for useful discussions. This work was pported by the Office of Naval Research under Contract 00014-86-K-0530 and by the Defence Advanced Research oject Agency and the Office of Naval Research under a contract from Texas Instruments on Contract N00014-87-0363/TI.

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ONTE CARLO ESTIMATES OF INCIDENCE F BASIC ACCESS ISDN GENERATED EMI

Monte Carlo simulations of basic access ISDN generated EMI to AM medium-wave reception in terraced-style buildings predict that unacceptably high incidences of interference will occur when the existing CCITT layer 1 specification is used for the ISDN design. A practical tightening of the specification provides large predicted improvements.

n recent years, concern has been expressed[1–3] that at customer premises, basic access integrated services digital etwork (ISDN) systems will generate high levels of electromagnetic interference (EMI) to AM receivers. The issue has alled into question the adequacy of the current CCITT user–etwork interface (UNI) specifications[6] to provide satisfactory MC performance for systems operating on conventional ustomer-premises pair cable. The present report provides ome estimates, derived by Monte Carlo simulation, that indicate both the likely severity of the problem and the degree of improvement to be expected by a practical tightening of the UNI specifications.

The simulation model is characterised as follows:

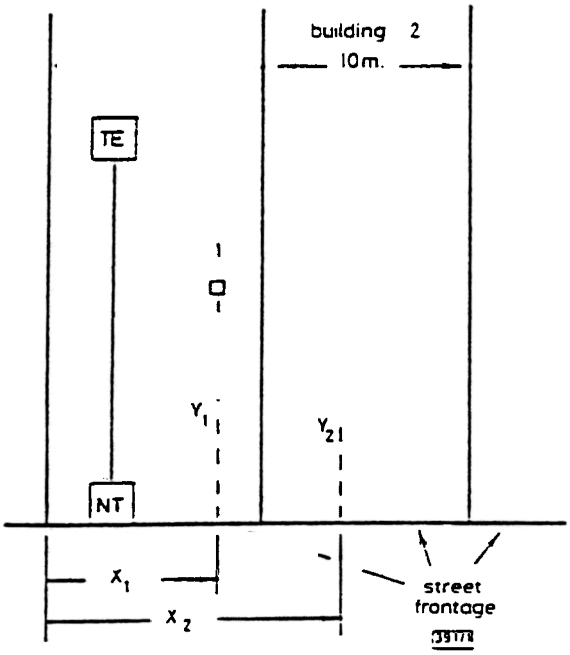

Fig. 1 *Terrace model layout: plan view*

possibility of adjacent building receivers on both sides of building 1 is not considered). Each receiver is at ground level, but is otherwise randomly located, with the *x* co-ordinates uniformly distributed between the limits set by the building side walls, and the *y* co-ordinates uniformly distributed over 0–12 metres.

(*b*) *ISDN system:* The system is of the simplest form, with a single TE unit coupled to the NT unit by a four-wire single quad cable, according to the layout of Fig. 2. Both the NT

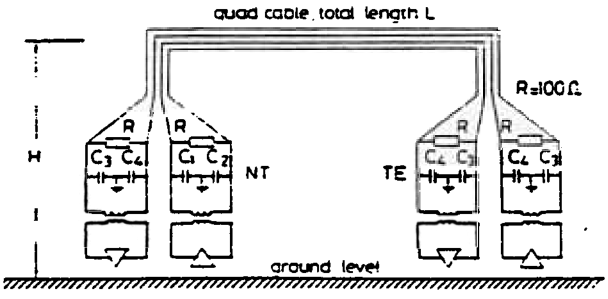

Fig. 2 *Assumed ISDN system model*

and TE units are modelled as directly earthed to ground. In reality the equipment will be RF earthed to the electric mains wiring, which will therefore carry common (or antenna) mode currents of the potential interfering signal (it is assumed that most installations will have at least one mains-powered TE unit). Consequently, the mains wiring is likely to contribute as much to the interfering field at the receiver as the ISDN bus cable. To approximately account for this situation, the height chosen for the cable of the model (see Fig. 2) has been made to depend on the assumed heights of both the actual cable and the mains wiring. Assumed levels of ground floor floor, ground floor ceiling and first floor ceiling are 0·5, 3·5 and 7 m above ground, respectively. The ISDN bus cable is run with equal probability at any one of these levels (L1, say). The electric mains cable is similarly run at any of these levels (L2). *H* in Fig. 2 is then chosen such that if L1 and L2 both equal 0·5, $H = 0{\cdot}5$ m; if L1 or L2 equals 7 m, $H = 7$ m; otherwise $H = 3{\cdot}5$ m.